

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-16 and 19-24 are presently active in this case, Claims 17 and 18 have been previously canceled without prejudice, and Claims 1, 8 and 9 are amended.

The amendment of Claim 1 finds non-limiting support in Applicants' specification as originally filed, for example from page 30, lines 10-14. Further, the amendments of Claims 8 and 9 are merely formal in nature. Therefore, the amendments are not believed to raise a question of new matter.

In the outstanding Official Action, Claims 1-5, 7-10, 13, 19 and 20 were rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 7,096,406 to Kanazawa et al. (hereinafter "Kanazawa"); Claims 6 and 12 were rejected under 35 U.S.C. §103(a) as unpatentable over Kanazawa in view of USP 6,339,546 to Katayama et al. (hereinafter "Kayatama"); and Claims 11, 14-16 and 21-24 were objected to as dependent upon a rejected base claim, but were indicated as being allowable if rewritten in independent form.

Applicants acknowledge with appreciation the indication of allowable subject matter in Claims 11, 14-16 and 21-24. However, Claims 11, 14-16 and 21-24 are presently maintained in dependent form, because Applicants believe that Claim 1 as currently amended includes allowable subject matter as discussed below.

First, Claim 1 recites, *inter alia*, "... a write-enable signal indicating that data is being written into the memory, ..." and "the data-path circuit outputs the write data to the memory in synchronization with a first clock signal ***generated from the write-enable signal.***"

Instead, Kanazawa describes "The above supply of data for writing and ECC data to the multilevel cell memory 3 is performed in synchronization with ***the system clock***" (Kanazawa at col. 10, lines 65-67, emphasis added) and "An ECC control circuit 50, provided

within the memory controller, *generates the internal clock CLK in synchronization with the system clock*; data supplied in synchronization with this clock CLK is transferred to the memory device” (Kanazawa at col. 12, lines 44-48, emphasis added). That is, Kanazawa only describes that the write data is transferred to the memory device in synchronization with *a system clock or a clock generated from the system clock*. Kanazawa does not teach or even suggest outputting write data to the memory device in synchronization with *a clock signal generated from a write-enable signal*, which indicates that data is being written into the memory device.

Thus, Kanazawa fails to disclose “... a write-enable signal indicating that data is being written into the memory, ...” and “the data-path circuit outputs the write data to the memory in synchronization with a first clock signal *generated from the write-enable signal*,” as recited in Claim 1.

Moreover, Claim 1 is amended to further recite “an enable interface circuit *which receives, from the host, a write-enable signal indicating that data is being written into the memory*, the enable interface circuit outputting the write-enable signal to the memory” and “the enable interface circuit does not output, to the memory, the write-enable signal when the write-enable signal is unnecessary for the memory.”

The outstanding Office Action indicates that Kanazawa at col. 3, lines 34-41 and col. 12, lines 44-49 discloses an enable interface circuit (Office Action at page 4, lines 17-18).

However, Kanazawa at col. 3, lines 34-41 and col. 12, lines 44-49 only describes that the write data is supplied to the ECC circuits and is provided to the memory in synchronization with the clock; an ECC control circuit 50 generates the internal clock CLK in synchronization with the system clock; and data supplied in synchronization with this clock CLK is transferred to the memory device. Kanazawa does not disclose that the memory controller 2 receives, from the host 1, a write-enable signal indicating that data is being

written into the cell memory 3. Further, Kanazawa does not disclose that the memory controller 2 does not output to the cell memory 3 the write-enable signal when the write-enable signal is unnecessary for the cell memory 3.

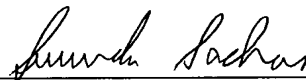
Thus, Kanazawa fails to disclose "an enable interface circuit which receives, from the host, a write-enable signal indicating that data is being written into the memory, the enable interface circuit outputting the write-enable signal to the memory" and "the enable interface circuit does not output, to the memory, the write-enable signal when the write-enable signal is unnecessary for the memory," as recited in Claim 1.

Accordingly, independent Claim 1 patentably distinguishes over Kanazawa. Since Claims 2-10, 12, 13, 19 and 20 are dependent directly or indirectly from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Therefore, presently active Claims 1-16 and 19-24 are believed to be allowable.

Consequently, in view of the present amendment and in light of the above discussions, it is believed that the outstanding rejection is overcome, and the application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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